67,200-1158
2002-1345

ANTI-FUSE STRUCTURE EMPLOYING METAL SILICIDE/DOPED POLYSILICON LAMINATE

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The invention relates generally to anti-fuse structures employed for fabricating microelectronic products. More particularly, the invention relates to anti-fuse structures with enhanced performance, as employed for fabricating microelectronic products.

2. Description of the Related Art

[0002] Anti-fuse structures are common in the microelectronic product fabrication art. In contrast to fuses, they provide programmable elements that allow for forming a conductive interconnect structure from a non-conductive interconnect structure. Typically, they are programmed employing an electrical programming voltage that is generally higher than an electrical circuit operating voltage. Anti-fuse structures find use in field programmable microelectronic memory and logic products where it is desirable for a user to program specific components into a specific electrical circuit to provide unique operating characteristics of the electrical circuit.

[0003] Although highly desirable in the microelectronic product fabrication art, anti-fuse structures are nonetheless not entirely without problems. In that regard, anti-fuse structures

are often difficult to fabricate with enhanced performance. It is towards the foregoing object that the invention is directed.

SUMMARY OF THE INVENTION

[0004] A first object of the invention is to provide an anti-fuse structure and a method for fabricating the anti-fuse structure.

[0005] A second object of the invention is to provide the anti-fuse structure and the method for fabricating the anti-fuse structure in accord with the first object of the invention, where the anti-fuse structure is fabricated with enhanced performance.

[0006] In accord with the objects of the invention, the invention provides an anti-fuse structure and a method for fabricating the anti-fuse structure.

[0007] In accord with the invention, the anti-fuse structure comprises a substrate having formed therein a contact region. The anti-fuse structure also comprises a metal silicide layer formed over and electrically connected with the contact region. The anti-fuse structure further comprises: (1) a first doped polysilicon layer formed upon the metal silicide layer; (2) an anti-fuse material layer formed upon the first doped polysilicon layer; and (3) a second doped polysilicon layer formed upon the anti-fuse material layer.

[0008] The anti-fuse structure of the invention may further comprises a conductor barrier layer formed interposed between the contact region and the metal silicide layer. Absent from the

anti-fuse structure of the invention is a doped polysilicon layer formed interposed between the contact region and the metal silicide layer.

[0009] The anti-fuse structure of the invention contemplates a method for fabricating the anti-fuse structure of the invention.

[0010] The invention provides an anti-fuse structure with enhanced performance and a method for fabricating the anti-fuse structure.

[0011] The invention realizes the foregoing object within the context of an anti-fuse structure comprising a metal silicide layer having formed thereupon a first doped polysilicon layer in turn having formed thereupon an anti-fuse material layer finally in turn having formed thereupon a second doped polysilicon layer. Within the anti-fuse structure, the metal silicide layer provides for a lower resistance of the anti-fuse structure when fused, and thus enhanced performance of the anti-fuse structure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] The objects, features and advantages of the invention are understood within the context of the Description of the Preferred Embodiment, as set forth below. The Description of the Preferred Embodiment is understood within the context of the accompanying drawings, which form a material part of this disclosure, wherein:

[0013] Fig. 1, Fig. 2, Fig. 3 and Fig. 4 show a series of schematic cross-sectional diagrams illustrating the results of

progressive stages in forming an anti-fuse structure within a microelectronic product in accord with the invention.

[0014] Fig. 5 shows a schematic cross-sectional diagram of operation of the anti-fuse structure in accord with the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

[0015] The invention provides an anti-fuse structure with enhanced performance and a method for fabricating the anti-fuse structure.

[0016] The invention realizes the foregoing object within the context of an anti-fuse structure comprising a metal silicide layer having formed thereupon a first doped polysilicon layer in turn having formed thereupon an anti-fuse material layer finally in turn having formed thereupon a second doped polysilicon layer. Within the anti-fuse structure, the metal silicide layer provides for a lower resistance of the anti-fuse structure when fused, and thus enhanced performance of the anti-fuse structure.

[0017] Fig. 1 to Fig. 4 show a series of schematic cross-sectional diagrams illustrating the results of progressive stages in forming an anti-fuse structure within a microelectronic product in accord with a preferred embodiment of the invention. Fig. 1 shows a schematic cross-sectional diagram of the microelectronic product at an early stage in its fabrication in accord with the preferred embodiment of the invention. Within

the following figures, a substrate 10 is provided as a horizontal reference plane upon and over which additional layers or structures are formed, whether or not the substrate is eventually employed in a horizontal disposition.

[0018] Fig. 1 first shows the substrate 10 having formed therein a contact region 12.

[0019] The substrate 10 may be employed within a microelectronic product selected from the group including but not limited to integrated circuit products (including in particular semiconductor products), ceramic substrate products and optoelectronic products. Preferably, the substrate 10 comprises a semiconductor substrate having formed therein semiconductor devices whose selective interconnection may be effected employing an anti-fuse structure in accord with the invention.

[0020] The contact region 12 may be a conductor contact region (i.e., formed employing a conductor including but not limited to a metal, metal alloy, doped polysilicon (having a dopant concentration of from about 1E18 to about 1E22 dopant atoms per cubic centimeter) or metal silicide (doped polysilicon/metal silicide stack)) conductor. Alternatively, the contact region 12 may be a semiconductor contact region formed employing a semiconductor material including but not limited to less highly doped silicon, germanium and silicon-germanium alloy semiconductor materials (i.e., from about 1E14 to about 1E16 dopant atoms per cubic centimeter).

[0021] Fig. 1 also shows a series of blanket layers formed upon the substrate 10 having formed therein the contact region 12.

[0022] The series of blanket layers comprises: (1) a blanket conductor barrier layer 14 formed upon the substrate 10 having formed therein the contact region 12; (2) a blanket metal silicide forming metal layer 16 formed upon the blanket conductor barrier layer 14; (3) an optional blanket undoped polysilicon layer 18 formed upon the blanket metal silicide forming metal layer 16; and (4) a blanket first doped polysilicon layer 20 of a first polarity formed upon the optional blanket undoped silicon layer 18.

[0023] The blanket conductor barrier layer 14 may be formed of conductor barrier materials as are conventional in the microelectronic product fabrication art, including but not limited to nitrides of metal silicide forming metals such as but not limited to titanium, tungsten, cobalt, nickel, platinum, vanadium and molybdenum. The blanket conductor barrier layer 14 may be formed employing methods as are conventional in the art, to provide the blanket conductor barrier layer 14 of thickness from about 50 to about 500 angstroms. Preferably, the blanket conductor barrier layer 14 is formed of a titanium nitride conductor barrier material formed to a thickness of from about 100 to about 200 angstroms.

[0024] The blanket metal silicide forming metal layer 16 may, as noted above, be formed of a metal silicide forming metal employed for forming the blanket conductor barrier layer 14.

Such metal silicide forming metals may be selected from the group including but not limited to titanium, tungsten, cobalt, nickel, platinum, vanadium and molybdenum. Typically, the blanket metal silicide forming metal layer 16 is formed to a thickness of from about 100 to about 500 angstroms. Preferably, the blanket metal silicide forming metal layer 16 is formed of titanium.

[0025] The optional blanket undoped silicon layer 18 may be formed of an amorphous undoped silicon material or a polycrystalline undoped silicon material. Typically, the optional blanket undoped silicon layer 18 is formed of a polycrystalline undoped silicon material formed to a thickness such as to provide for complete consumption of the blanket undoped silicon layer 18 when forming a metal silicide layer therefrom incident to thermal annealing with the blanket metal silicide forming metal layer 16. Typically the thickness will be from about 100 to about 500 angstroms.

[0026] Finally, the blanket first doped polysilicon layer 20 is formed of a doped polysilicon material as is otherwise conventional in the art, and formed with a first dopant polarity and a first dopant concentration. The first dopant polarity may be either an N polarity of a P polarity. The first dopant concentration may be either a - dopant concentration or a + dopant concentration. Preferably, the blanket first doped polysilicon layer 20 is formed with a P dopant polarity and a + dopant concentration (i.e., from about 1E20 to about 1E22 dopant atoms per cubic centimeter).

[0027] Fig. 2 first shows the results of thermally annealing the microelectronic product of Fig.1 to form from the blanket metal silicide forming metal layer 16 and the blanket undoped silicon layer 16 (if present) a blanket metal silicide layer 17. Since the blanket metal silicide forming metal layer 16 is formed upon the blanket barrier layer 14, the thermal annealing proceeds such that a doped polysilicon layer is neither formed nor remains interposed between the blanket metal silicide layer 17 and the blanket barrier layer 14 or the contact region 12. Such thermal annealing also partially (and minimally) consumes the blanket first doped polysilicon layer 20 to form a partially consumed blanket first doped polysilicon layer 20'. When the blanket undoped silicon layer 18 is absent, the blanket metal silicide layer 17 is formed in conjunction with an enhanced consumption of the blanket first doped polysilicon layer 20. The use of the optional blanket undoped silicon layer 18 is desirable since the same provides for limited doping of the blanket metal silicide layer 17. The thermal annealing is undertaken at a temperature and for a time period appropriate for a metal silicide forming metal from which is formed the blanket metal silicide forming metal layer 16. Typically, the thermal annealing is undertaken at a temperature of from about 900 to about 1100 degrees centigrade and a rapid thermal annealing (i.e., thermal annealing temperature rise of from about 0.5 to about 2.0 seconds) time period of from about 0.5 to about 2.0 minutes, particularly when the blanket metal silicide forming metal layer 16 is formed of a titanium metal silicide forming metal.

[0028] Fig. 3 first shows the results of sequentially patterning the partially consumed blanket first doped polysilicon

layer 20', the blanket metal silicide layer 17 and the blanket barrier layer 14 to form a corresponding series of patterned layers comprising a patterned first doped polysilicon layer 20a aligned upon a patterned metal silicide layer 17a in turn aligned upon a patterned barrier layer 14a.

[0029] The foregoing patterning may be effected while employing etch methods as are conventional in the microelectronic product fabrication art, and as are appropriate to the materials from which are formed the partially consumed blanket first doped polysilicon layer 20', the blanket metal silicide layer 17 and the blanket barrier layer 14. Although the etch methods may include wet chemical etch methods and dry plasma etch methods, anisotropic dry plasma etch methods are preferred.

[0030] Fig. 3 also shows the results of forming a pair of patterned planarized first dielectric layers 22a and 22b adjoining a pair of sidewalls of the stack comprising the patterned barrier layer 14a, the patterned metal silicide layer 17a and the patterned first doped polysilicon layer 20a.

[0031] The pair of patterned planarized first dielectric layers 22a and 22b may be formed employing methods and materials as are otherwise generally conventional in the microelectronic product fabrication art. Typically and preferably, the pair of patterned planarized first dielectric layers 22a and 22b is formed of a silicon oxide material formed employing a high density plasma chemical vapor deposition (HDP-CVD) method and planarized employing a chemical mechanical polish (CMP) planarizing method while employing the patterned first doped

polysilicon layer 20a as a planarizing stop layer. Other methods and materials may also be employed.

[0032] Fig. 4 first shows a blanket anti-fuse material layer 24 formed upon the microelectronic product of Fig. 3, including the pair of patterned planarized first dielectric layers 22a and 22b and patterned first doped polysilicon layer 20a.

[0033] The blanket anti-fuse material layer may be formed of anti-fuse materials as are conventional in the microelectronic product fabrication art. Such anti-fuse materials may include, but are not limited to amorphous silicon or amorphous carbon anti-fuse materials, as well as more conventional dielectric anti-fuse materials, such as but not limited to silicon oxide, silicon nitride and silicon ox nitride dielectric anti-fuse materials. Preferably, the blanket anti-fuse material layer 24 is formed at least in part of a silicon oxide anti-fuse material, formed to a thickness of from about 10 to about 50 angstroms.

[0034] Fig. 4 also shows a patterned second doped polysilicon layer 26 formed upon the blanket anti-fuse material layer 24 and nominally centered above the patterned first doped polysilicon layer 20a. Analogously with the patterned first doped polysilicon layer 20a, the patterned second doped polysilicon layer 26 may also be formed of either dopant polarity (i.e., N or P) or either dopant concentration (i.e., - or +). The present invention provides particular value, however, under circumstances where the patterned second doped polysilicon layer 26 is formed of an N polarity and a - dopant concentration (i.e., from about 1E15 to about 1E17 dopant atoms per cubic centimeter) under

circumstances where the patterned first doped polysilicon layer 24a is formed of a P+ polarity (or an analogous bilateral complementary dopant polarity and concentration ordering). Under such circumstances, an anti-fuse structure of the invention when fused provides a diode conductor structure rather than a pure conductor structure.

[0035] Fig. 5 shows a schematic cross-sectional diagram illustrating operation of the anti-fuse structure of Fig. 4.

[0036] As is illustrated in Fig. 5, incident to use of a proper programming voltage and programming current, the patterned first doped polysilicon layer 20a and the patterned second doped polysilicon layer 26 fuse to form a fused patterned first doped polysilicon layer 20a' and a fused patterned second doped polysilicon layer 26', while simultaneously forming a pair of patterned anti-fuse material layers 24a and 24b from the blanket anti-fuse material layer 24. In accord with the above disclosure, when each of the patterned first doped polysilicon layer 20a and the patterned second doped polysilicon layer 26 is of the same dopant polarity, the anti-fuse structure of Fig. 4 is fused to form a fused conductor interconnect structure. In contrast, when each of the patterned first doped polysilicon layer 20a and the patterned second doped polysilicon layer 26 is formed of opposite dopant polarity, the anti-fuse structure of Fig. 4 is fused to form an anti-fuse diode structure.

[0037] The invention provides an anti-fuse structure with enhanced performance. The invention realizes the foregoing object by employing a metal silicide layer within the anti-fuse

structure, and by forming upon, and not beneath, the metal silicide layer a doped polysilicon layer. The metal silicide layer with the doped polysilicon layer formed thereupon but not therebeneath provides decreased anti-fuse electrical resistance when fused. The anti-fuse structure may also be formed employing a simple manufacturing process with a minimal number of doped polysilicon layers. The minimal number of doped polysilicon layers provides that the anti-fuse structure may further be fabricated employing simplified etch methods and chemical mechanical polish planarization methods when forming the anti-fuse structure.

[0038] The preferred embodiment of the invention is illustrative of the invention rather than limiting of the invention. Revisions and modifications may be made to materials, structures and dimensions in accord with the preferred embodiment of the invention while still providing an embodiment in accord with the invention, further in accord with the accompanying claims.